

TSK82N25M

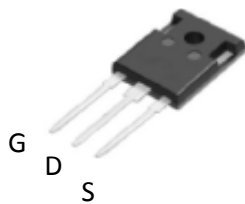
250V N-Channel MOSFET

General Description

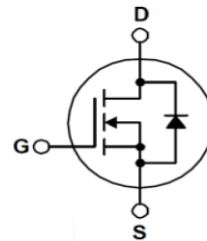
This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high power inverter, cutting machine.

Features

- 82A, 250V, Max. $R_{DS(on)} = 38m\Omega$ @ $V_{GS} = 10V$
- Low gate charge: $Q_g = 134nC$ (Typ.)
- 100% avalanche tested
- RoHS compliant device



TO-247



Absolute Maximum Ratings $T_c = 25^\circ C$ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DS}	Drain-Source Voltage		250	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Drain Current	$T_c = 25^\circ C$	82	A
		$T_c = 100^\circ C$	52	A
I_{DM}	Pulsed Drain Current	(Note 1)	328	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	3063	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	19.80	mJ
I_{AR}	Repetitive Avalanche current	(Note 1)	35	A
P_D	Power Dissipation ($T_c = 25^\circ C$)		198	W
T_J	Junction temperature		150	$^\circ C$
T_{stg}	Storage temperature range		-55~150	$^\circ C$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.63	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.50	$^\circ C/W$

Electrical Characteristics $T_c=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 41\text{ A}$	--	32	38	m Ω
g_{fs}	Forward transfer conductance	$V_{DS} = 15\text{ V}, I_D = 4.5\text{ A}$ (Note 4)	--	12	--	S

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	250	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=250\text{ V}, V_{GS} = 0\text{ V}$	--	--	25	μA
		$V_{DS} = 200\text{ V}, T_c = 125^{\circ}\text{C}$	--	--	100	μA
I_{GSS}	Gate leakage current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	± 100	nA
R_g	Internal gate resistance	Open drain, $f=1\text{ MHz}$	--	1	--	Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	6790	--	pF
C_{oss}	Output Capacitance		--	847	--	pF
C_{rss}	Reverse Transfer Capacitance		--	93	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DD}=125\text{ V}, I_D=82\text{ A},$ $R_G=25\Omega$	--	78	--	ns
t_r	Turn-On Rise Time		--	24	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	297	--	ns
t_f	Turn-Off Fall Time		--	90	--	ns
Q_g	Total Gate Charge	$V_{DS}=200\text{ V}, V_{GS}=10\text{ V},$ $I_D=82\text{ A}$	--	134	--	nC
Q_{gs}	Gate-Source Charge		--	44	--	nC
Q_{gd}	Gate-Drain Charge		--	56	--	nC

Source-Drain Diode Ratings and Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

I_S	Continuous Source-Drain Diode Forward Current		--	--	82	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	328	
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 82\text{ A}, V_{GS} = 0\text{ V}$	--	--	1.5	V
t_{rr}	Reverse recovery time (Note 3,4)	$I_S = 82\text{ A}, V_{GS} = 0\text{ V}$ $di_p/dt = 100\text{ A}/\mu\text{s}$	--	324	--	ns
Q_{rr}	Reverse recovery charge (Note 3,4)		--	21	--	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=4\text{ mH}$, $I_{AS}=35\text{ A}$, $V_{DD}=50\text{ V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Typical Characteristics Curve

Fig. 1 $I_D - V_{DS}$

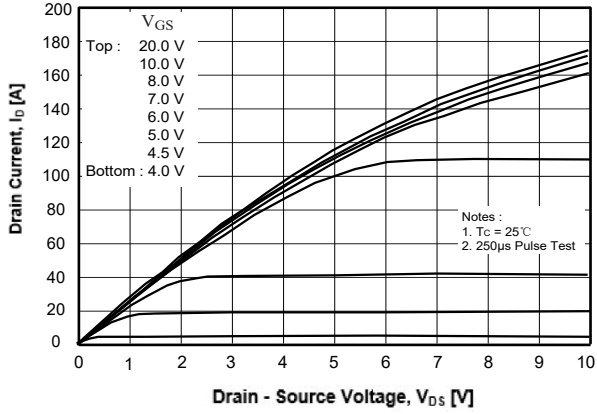


Fig. 2 $I_D - V_{GS}$

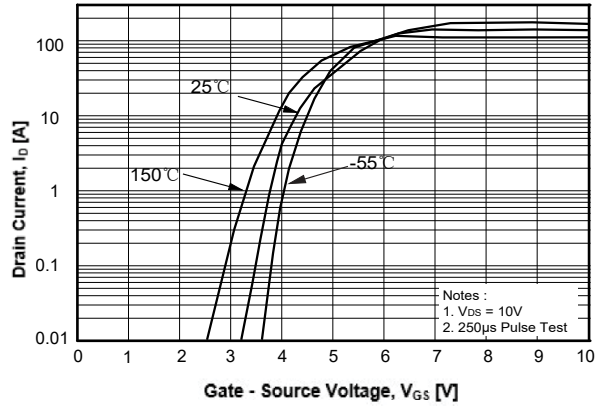


Fig. 3 $R_{DS(ON)} - I_D$

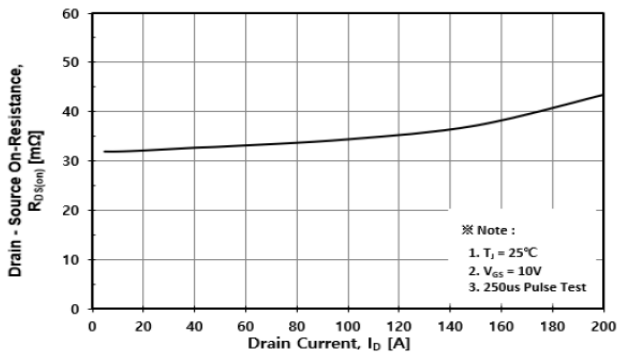


Fig. 4 $I_S - V_{SD}$

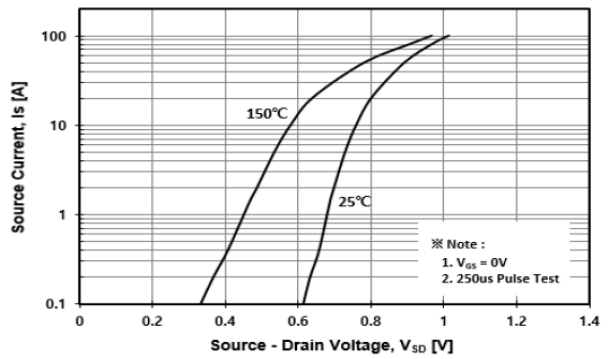


Fig. 5 Capacitance - V_{DS}

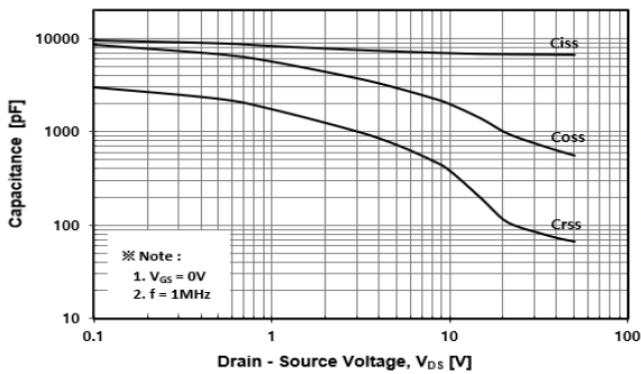
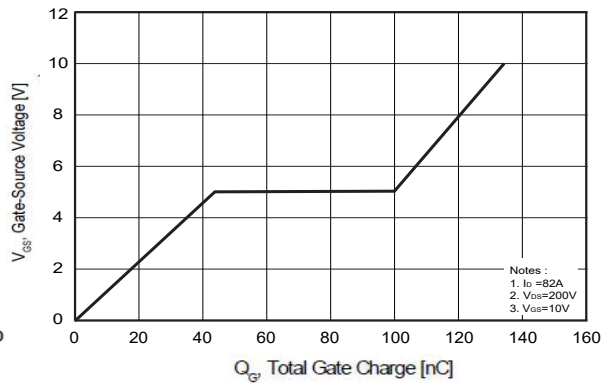


Fig. 6 $V_{GS} - Q_G$



Typical Characteristics Curve (Continue)

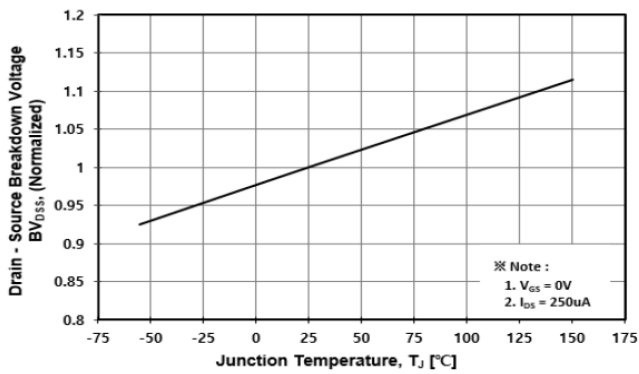
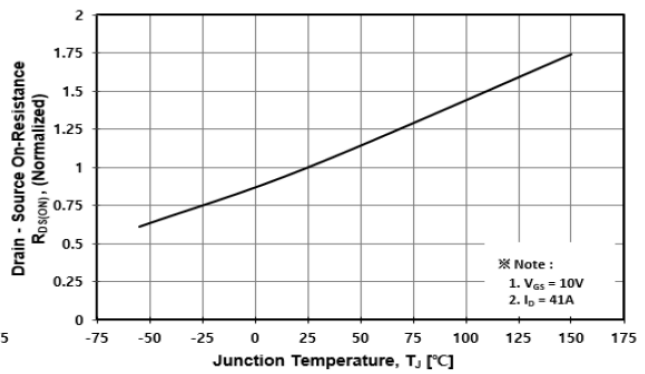
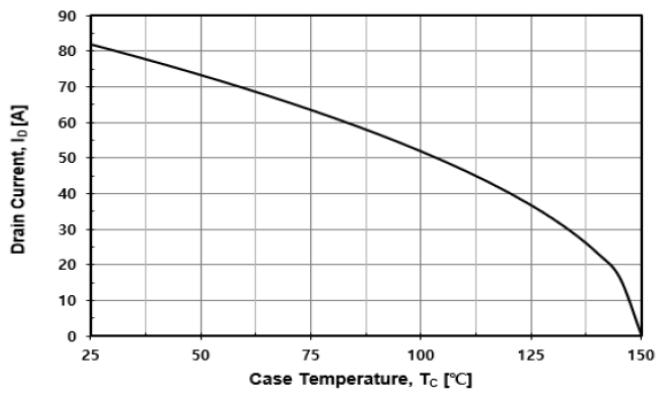
Fig. 7 $BV_{DS5} - T_J$ Fig. 8 $R_{DS(ON)} - T_J$ Fig. 9 $I_D - T_C$ 

Fig. 10 Safe Operating Area

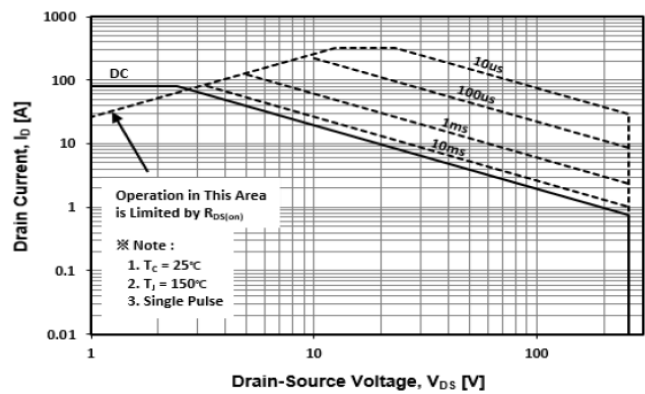


Fig. 11 Transient Thermal Impedance

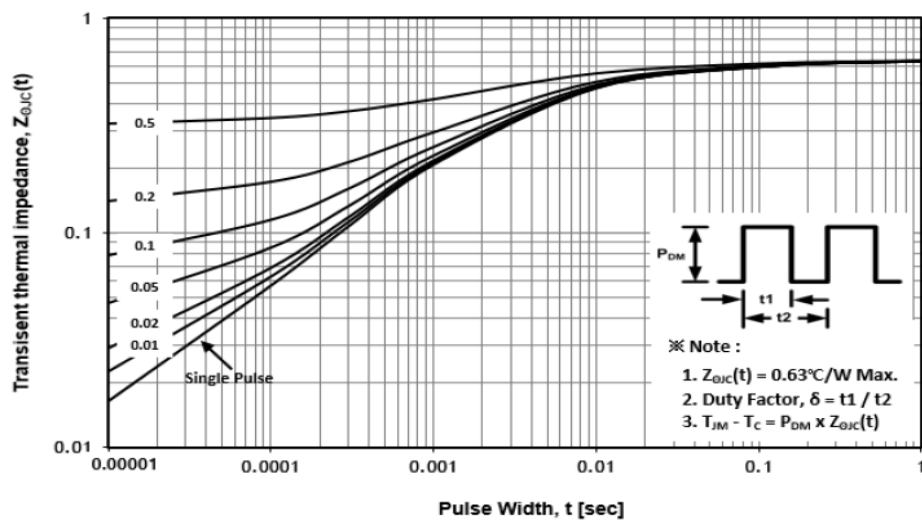


Fig. 12 Gate Charge Test Circuit & Waveform

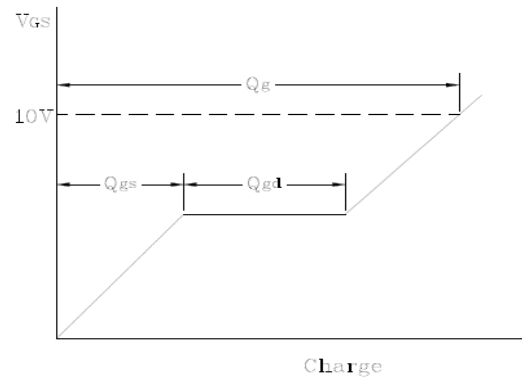
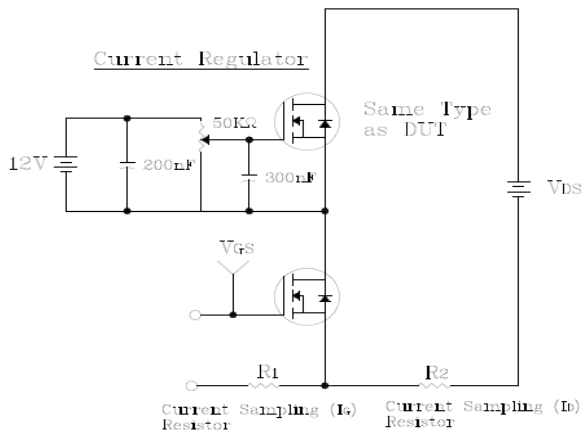


Fig. 13 Resistive Switching Test Circuit & Waveform

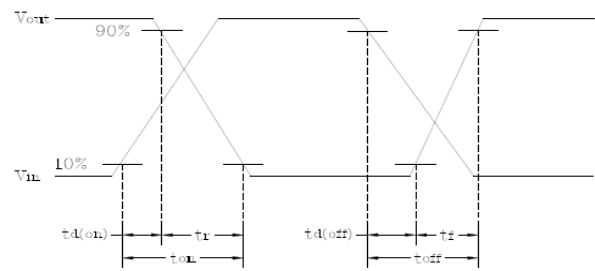
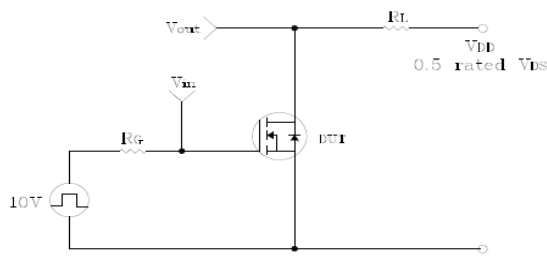


Fig. 14 E_{AS} Test Circuit & Waveform

