

TSA82N25M

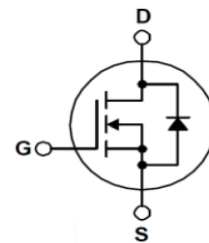
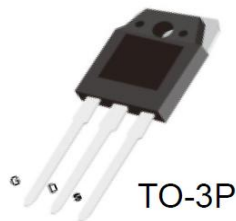
250V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high power inverter, cutting machine.

Features

- 82A, 250V, Max. $R_{DS(on)} = 38m\Omega$ @ $V_{GS} = 10V$
- Low gate charge: $Q_g = 134nC$ (Typ.)
- 100% avalanche tested
- RoHS compliant device



Absolute Maximum Ratings $T_c = 25^\circ C$ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		250	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Drain Current	$T_c = 25^\circ C$	82	A
		$T_c = 100^\circ C$	52	A
I_{DM}	Pulsed Drain Current	(Note 1)	328	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	3063	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	19.80	mJ
I_{AR}	Repetitive Avalanche current	(Note 1)	35	A
P_D	Power Dissipation ($T_c = 25^\circ C$)		198	W
T_J	Junction temperature		150	$^\circ C$
T_{stg}	Storage temperature range		-55~150	$^\circ C$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.63	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.50	$^\circ C/W$

Electrical Characteristics T_c=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 uA	2.0	--	4.0	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 41 A	--	32	38	mΩ
g _{fs}	Forward transfer conductance	V _{DS} = 15V, I _D = 4.5A (Note 4)	--	12	--	S

Off Characteristics

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 uA	250	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =250V, V _{GS} = 0 V	--	--	25	uA
		V _{DS} = 200 V, T _C = 125 °C	--	--	100	uA
I _{GSS}	Gate leakage current	V _{GS} =±20V, V _{DS} = 0 V	--	--	±100	nA
R _g	Internal gate resistance	Open drain, f=1MHz	--	1	--	Ω

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	6790	--	pF
C _{oss}	Output Capacitance		--	847	--	pF
C _{rss}	Reverse Transfer Capacitance		--	93	--	pF

Switching Characteristics

t _{d(on)}	Turn-On Time	V _{DD} =125V, I _D =82A, R _G =25Ω	--	78	--	ns
t _r	Turn-On Rise Time		--	24	--	ns
t _{d(off)}	Turn-Off Delay Time		--	297	--	ns
t _f	Turn-Off Fall Time		--	90	--	ns
Q _g	Total Gate Charge	V _{DS} =200V, V _{GS} =10V, I _D =82A	--	134	--	nC
Q _{gs}	Gate-Source Charge		--	44	--	nC
Q _{gd}	Gate-Drain Charge		--	56	--	nC

Source-Drain Diode Ratings and Characteristics (T_C=25°C unless otherwise noted)

I _S	Continuous Source-Drain Diode Forward Current		--	--	82	A
I _{SM}	Pulsed Source-Drain Diode Forward Current		--	--	328	
V _{SD}	Source-Drain Diode Forward Voltage	I _S = 82A, V _{GS} = 0 V	--	--	1.5	V
t _{rr}	Reverse recovery time (Note 3,4)	I _S = 82A, V _{GS} = 0 V di _p /dt = 100 A/μs	--	324	--	ns
Q _{rr}	Reverse recovery charge (Note 3,4)		--	21	--	uC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. L=4mH, I_{AS}=35A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. Pulse test: Pulse width ≤300us, Duty cycle ≤2%
4. Essentially independent of operating temperature typical characteristics

Typical Characteristics Curve

Fig. 1 $I_D - V_{DS}$

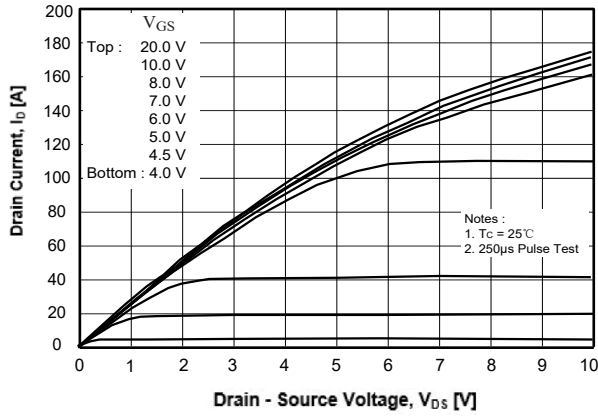


Fig. 2 $I_D - V_{GS}$

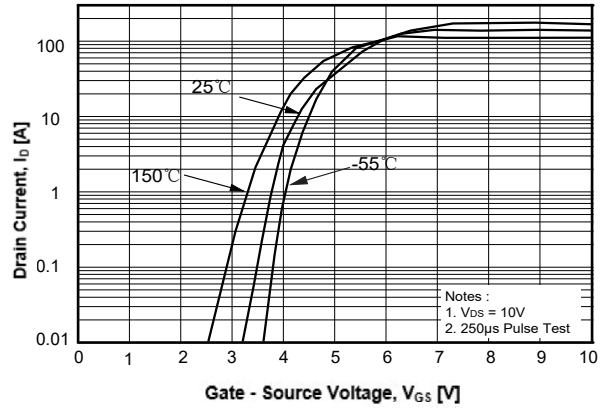


Fig. 3 $R_{DS(ON)} - I_D$

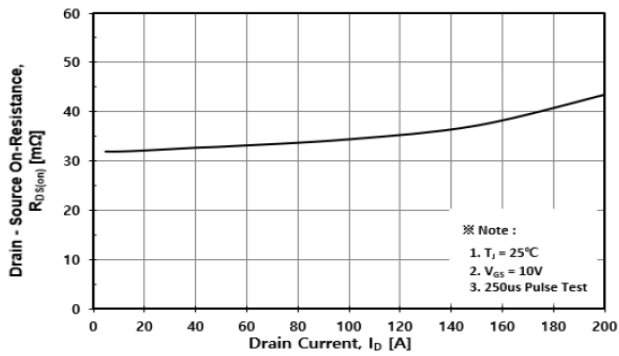


Fig. 4 $I_S - V_{SD}$

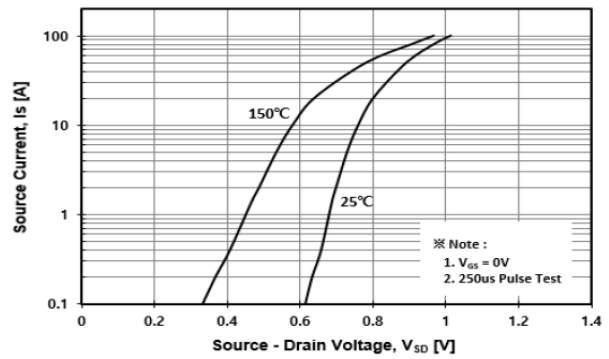


Fig. 5 Capacitance - V_{DS}

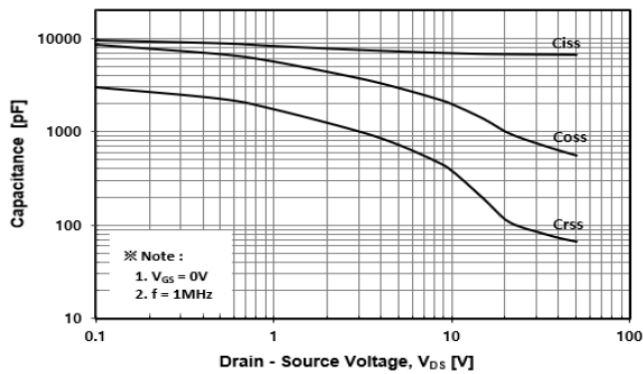
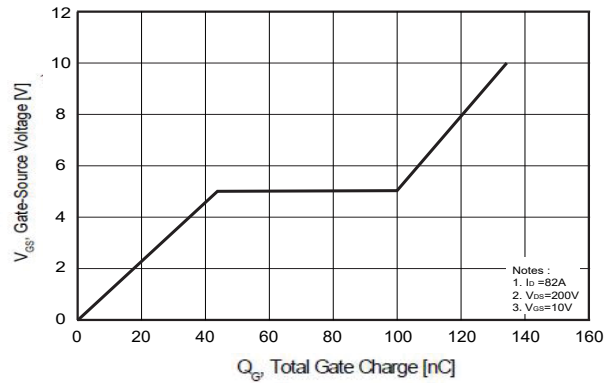


Fig. 6 $V_{GS} - Q_G$



Typical Characteristics Curve (Continue)

Fig. 7 $BV_{DSS} - T_J$

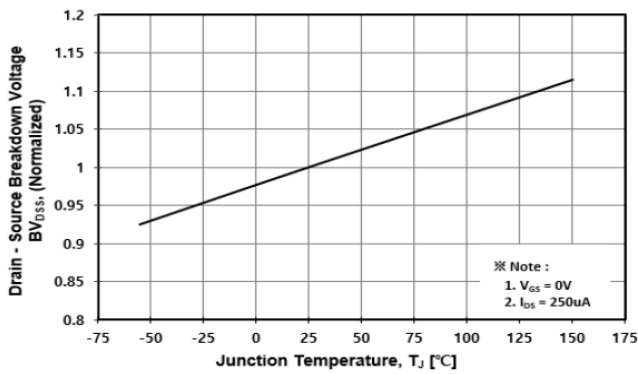


Fig. 8 $R_{DS(ON)} - T_J$

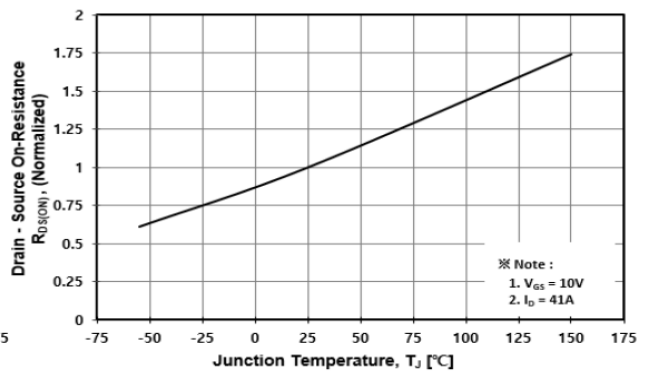


Fig. 9 $I_D - T_C$

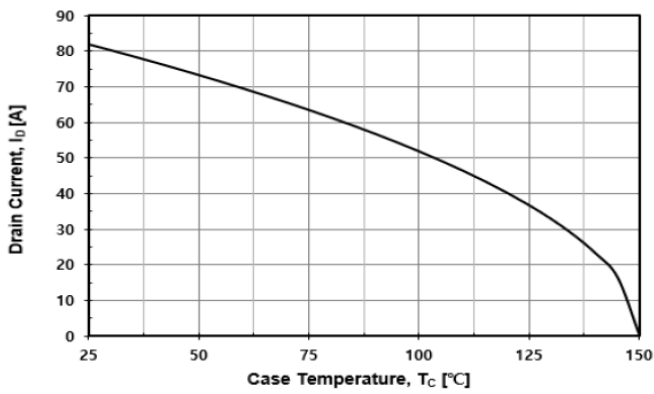


Fig. 10 Safe Operating Area

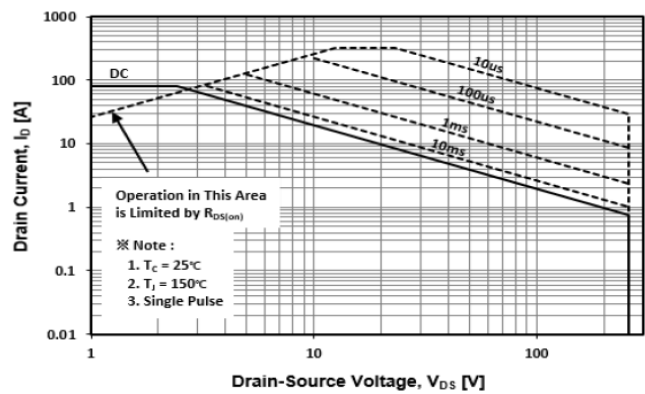


Fig. 11 Transient Thermal Impedance

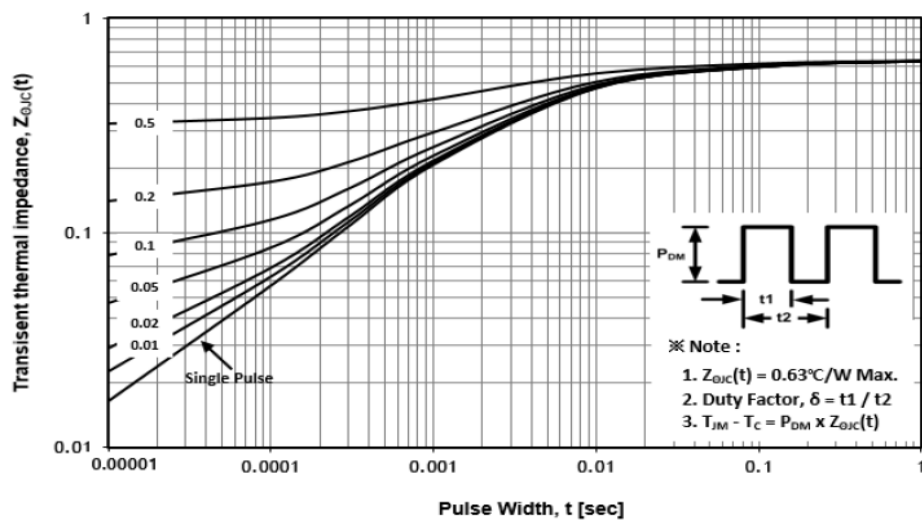


Fig. 12 Gate Charge Test Circuit & Waveform

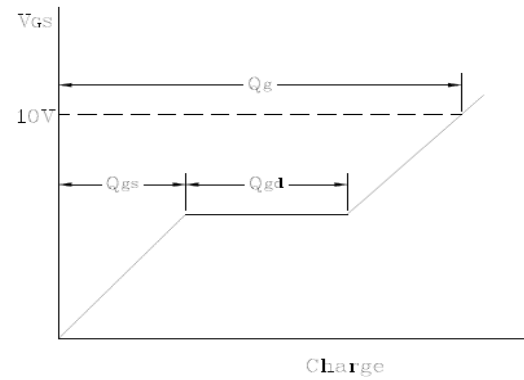
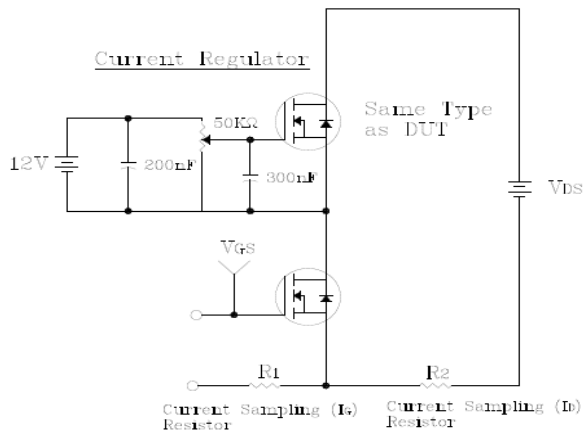


Fig. 13 Resistive Switching Test Circuit & Waveform

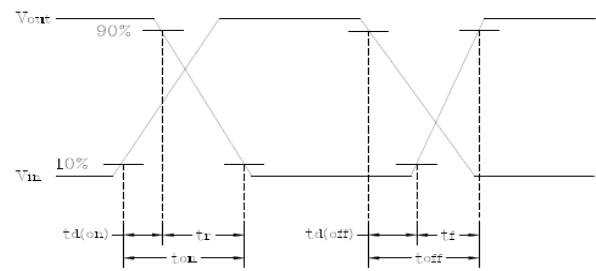
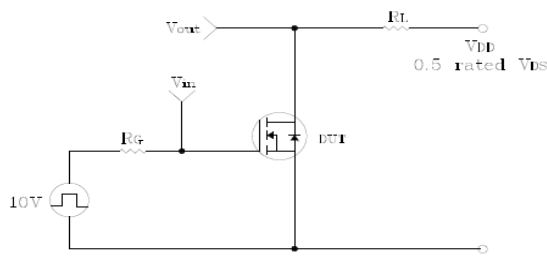


Fig. 14 E_{AS} Test Circuit & Waveform

