



TSF25N50MD

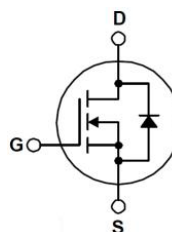
500V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 25A,500V,Max. $R_{DS(on)}$ =0.25 Ω @ V_{GS} =10V
- Low gate charge(typical 70nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

$T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DS}	Drain-Source Voltage		500	V
V_{GS}	Gate-Source Voltage		± 30	V
I_D	Drain Current	$T_C = 25^{\circ}\text{C}$	25	A
		$T_C = 100^{\circ}\text{C}$	13	A
I_{DM}	Pulsed Drain Current		80	A
E_{AS}	Single Pulsed Avalanche Energy	($L=0.4\text{mH}$)	900	mJ
P_D	Power Dissipation ($T_C = 25^{\circ}\text{C}$)		37	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^{\circ}\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	--	3.4	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	--	62.5	$^{\circ}\text{C/W}$

Electrical Characteristics $T_J=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	--	0.21	0.25	Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 150\text{ V}, T_J = 100\text{ }^{\circ}\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	3900	--	pF
C_{oss}	Output Capacitance		--	400	--	pF
C_{rss}	Reverse Transfer Capacitance		--	40	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 75\text{ V}, I_D = 25\text{ A},$ $R_G = 10\text{ }\Omega$	--	100	--	ns
t_r	Turn-On Rise Time		--	400	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	100	--	ns
t_f	Turn-Off Fall Time		--	100	--	ns
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 25\text{ A},$ $V_{GS} = 10\text{ V}$	--	70	--	nC
Q_{gs}	Gate-Source Charge		--	18	--	nC
Q_{gd}	Gate-Drain Charge		--	35	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I _S	Continuous Source-Drain Diode Forward Current		--	--	25	A
I _{SM}	Pulsed Source-Drain Diode Forward Current		--	--	80	
V _{SD}	Source-Drain Diode Forward Voltage	I _S = 25A, V _{GS} = 0 V	--	--	1.5	V
t _{rr}	Reverse Recovery Time	I _S =25A, V _{GS} = 0 V di _F /dt = 100 A/μs	--	500	--	ns
Q _{rr}	Reverse Recovery Charge		--	7.2	--	μC

Typical Characteristics

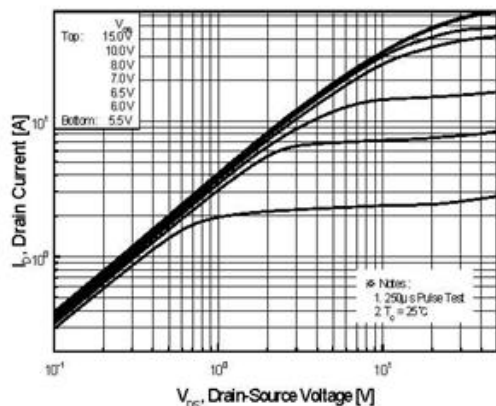


Figure 1. On-Region Characteristics

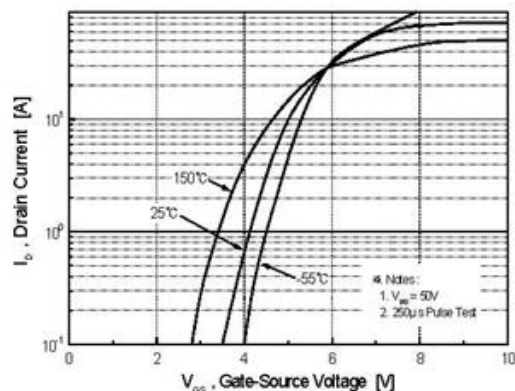


Figure 2. Transfer Characteristics

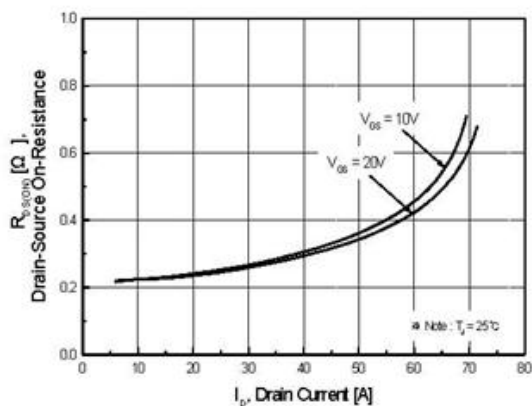


Figure 3. On-Resistance Variation vs

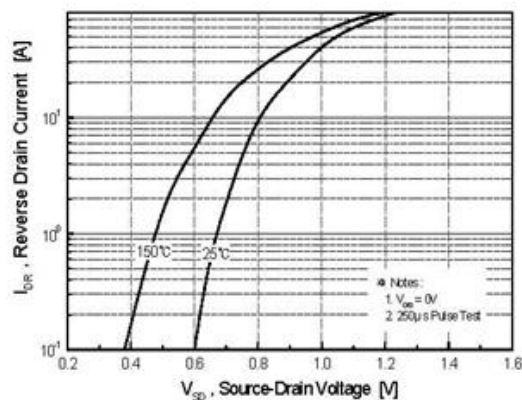


Figure 4. Body Diode Forward Voltage

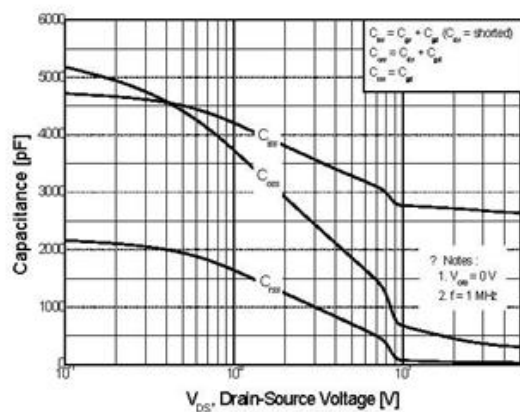


Figure 5. Capacitance Characteristics

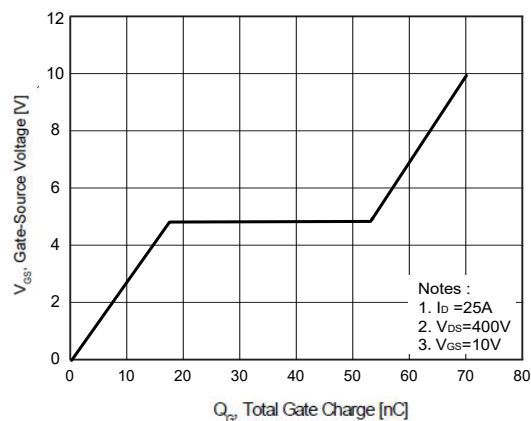


Figure 6. Gate Charge Characteristics

Typical Characteristics

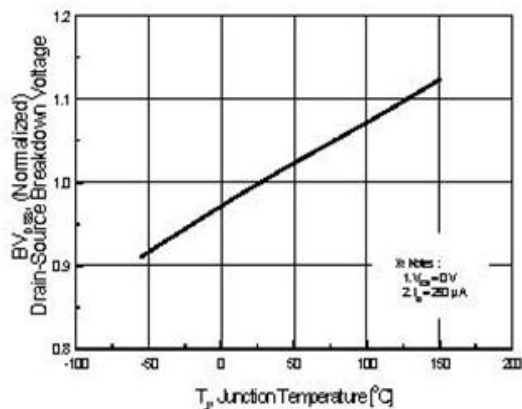


Figure 7. Breakdown Voltage Variation

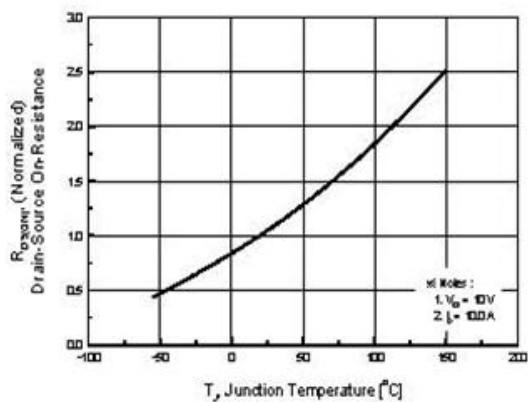


Figure 8. On-Resistance Variation

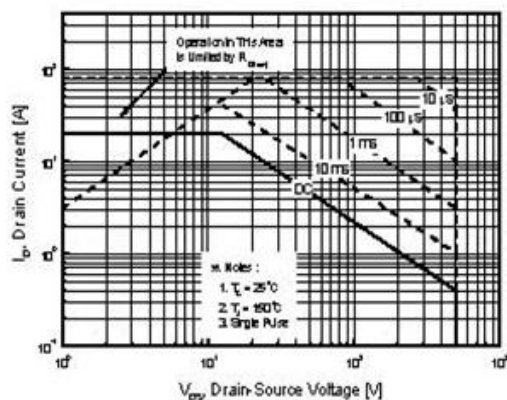


Figure 9. Maximum Safe Operating Area

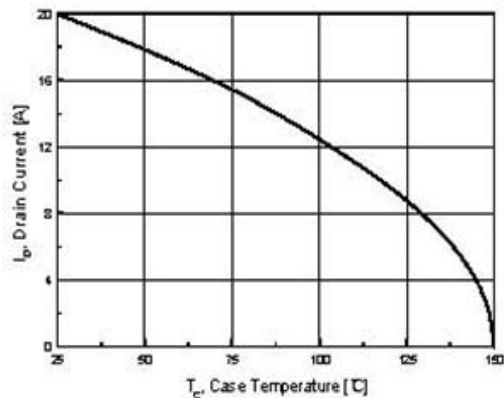


Figure 10. Maximum Drain Current vs Case Temperature

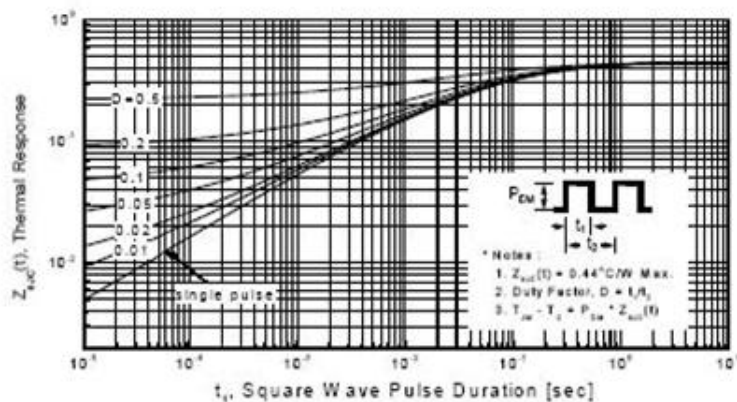


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

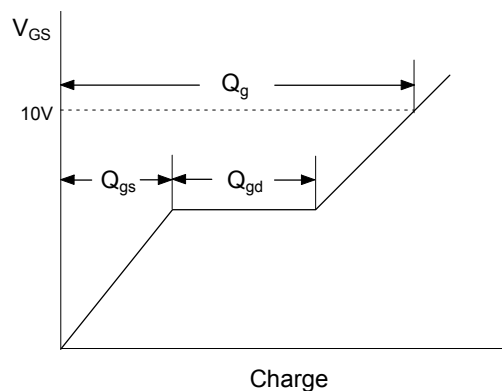
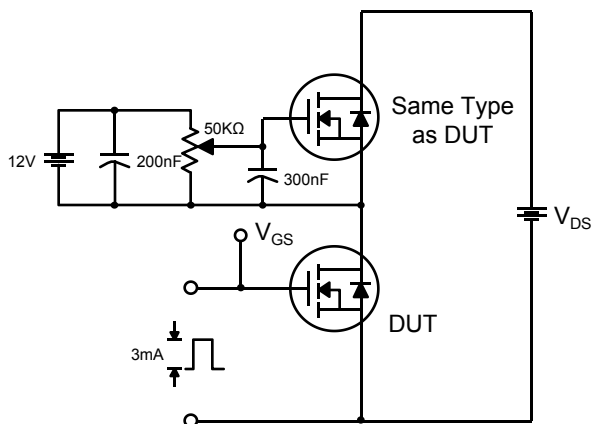


Fig 13. Resistive Switching Test Circuit & Waveforms

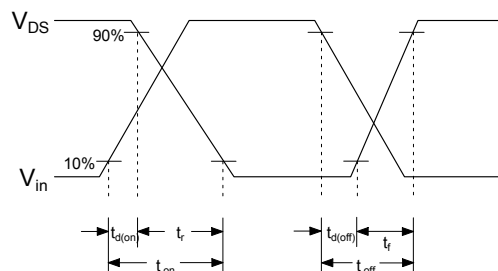
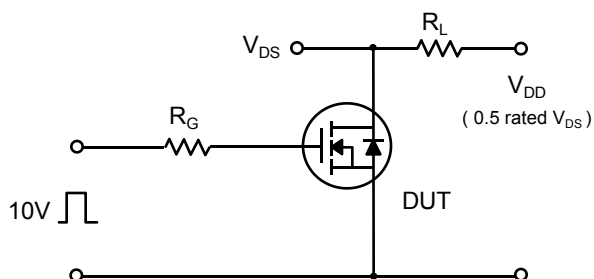


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

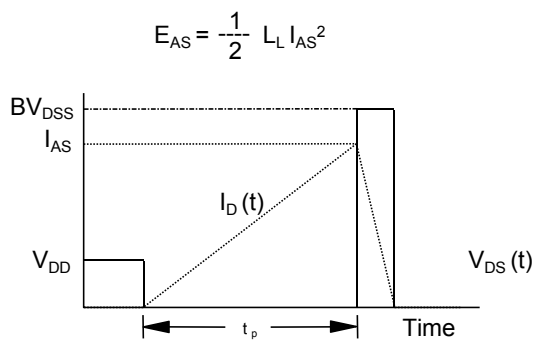
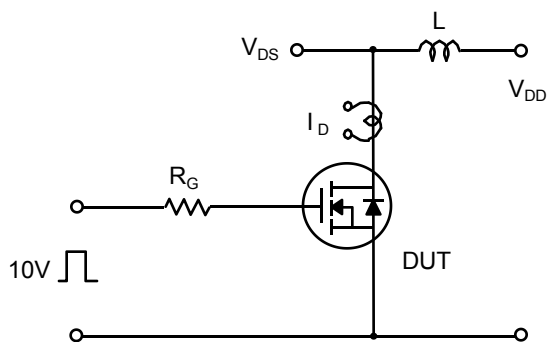


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

